REMARKS

Claims 1-21 are pending in the present application, and were rejected by the Examiner in an Office Action dated 11/04/02. Claims 1, 2, 4, 5, 8-12 and 15-~~18~~ 19 have been amended herewith. Reconsideration of the claims is respectfully requested. CEL 2/10/03

Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification.

I. Drawing Objection

The Examiner objected to the drawing as failing to comply with 37 CFR 1.84(p)(5), and states that certain reference sign(s) shown in the drawings are not mentioned in the description. Applicants have amended the description to mention the articulated reference signs. It should be noted, however, that with respect to reference signs 314, 316, 318 and 320 of Fig. 3, these reference signs are already mention in the description at page 13, line 26.

Applicants thus show that the objection to the drawing has been overcome by this amendment to the description.

II. Objection to Specification

The Examiner objected to the Specification, stating that the abstract was too long and also pointing out various informalities that needed correction. Applicants have amended the specification herewith to address the Examiner's concerns.

Applicants thus show that the objection to the specification has been overcome by this amendment to the specification.

III. Claim Objections

The Examiner objected to Claims 10 and 17 due to various informalities. Applicants have amended such claims as suggested by the Examiner. Applicants thus show that the objection to the claims has been overcome by such amendment.

IV. 35 U.S.C. § 112, Second Paragraph

The Examiner has rejected Claims 1, 8 and 15 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. This rejection is respectfully traversed.

Applicants have amended such claims to correct the antecedent bases issues cited by the Examiner. Therefore the rejection of Claims 1, 8 and 15 under 35 U.S.C. § 112, second paragraph has been overcome.

V. 35 U.S.C. § 103, Obviousness

A. The Examiner rejected Claims 1, 3, 8, 10, 15 and 17 under 35 U.S.C. § 103 as being unpatentable over Ahrens et al. (US 6,230,265 B1) in view of Berglund et al. (US 6,044,411). This rejection is respectfully traversed.

Regarding Claims 1, 8 and 15, such claims have been amended to recite that addresses used when accessing devices contained within said plurality of input/output drawers do not change when reconfiguring at least one of the input/output drawers within the data processing system. Support for this amendment is shown to be at least partially at Specification page 15, lines 1-19 and page 16, lines 16-24. None of the cited references teach or suggest this claimed feature, which addresses a problem of system configuration when drawers are inserted, removed or rearranged (Specification page 3, line 17 – page 4, line 1). Thus, it is shown that the rejection of Claims 1, 8 and 15 has been traversed.

Applicants traverse the rejection of dependent Claims 3, 10 and 17 for similar reasons to those given above with respect to independent Claims 1, 8 and 15.

Therefore, the rejection of Claims 1, 3, 8, 10, 15 and 17 under 35 U.S.C. § 103 has been overcome.

B. The Examiner rejected Claims 2, 9 and 16 under 35 U.S.C. § 103 as being unpatentable over Ahrens et al. (US 6,230,265 B1) in view of Berglund et al. (US 6,044,411) and further in view of Sidhu et al. (US 5,884,322). This rejection is

respectfully traversed for similar reasons to those given above regarding Claim 1, 8 and 15.

C. The Examiner rejected Claims 4, 6, 7, 11, 13, 14, 18, 20 and 21 under 35 U.S.C. § 103 as being unpatentable over Ahrens et al. (US 6,230,265 B1) in view of Berglund et al. (US 6,044,411) and Sidhu et al. (US 5,884,322), and further in view of Lortez et al. (US 6,041,364). This rejection is respectfully traversed for similar reasons to those given above regarding Claim 1, 8 and 15.

D. The Examiner rejected Claims 5, 12 and 19 under 35 U.S.C. § 103 as being unpatentable over Ahrens et al. (US 6,230,265 B1) in view of Berglund et al. (US 6,044,411) and Sidhu et al. (US 5,884,322), and further in view of Ahrens et al. (US 6,148,419). This rejection is respectfully traversed for similar reasons to those given above regarding Claim 1, 8 and 15.

Applicants further show that regarding the rejection of Claims 1-21 under 35 U.S.C. § 103, the Examiner is using improper hindsight analysis in rejecting such claims. When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. "...absence of such suggestion to combine is dispositive in an obviousness determination". *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573, 42 USPQ2d 1378 (Fed. Cir. 1997). The Examiner states that it would have been obvious to have included first and second means, as disclosed by Berglund, in said computer product, as disclosed by Ahren '265, for the advantage of providing said unique location identifier is (sic) instantly available to an operating system when a logical addresses (sic) are assigned thereby. Applicants show, however, that Ahren requires that I/O drawers by installed sequentially (Col. 4, lines 57-62) to provide a known system configuration, so there would be no reason or motivation to include physical location determination teachings from Berglund. The only motivation for such combination comes from Applicants' own invention, which is improper hindsight analysis. It is error to reconstruct the patentee's claimed invention from the prior art by using the patentee's

claims as a "blueprint". When prior art references require selective combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight obtained from the invention itself. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985). Hence, the rejection of Claims 1-21 is further traversed.

VI. Conclusion

It is respectfully urged that the subject application is patentable over the cited references, and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 2/3/03

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APPENDIX
(REDLINE VERSION TO SHOW CHANGES MADE)

Amended paragraph commencing on page 8, line 2:

Thus, for example, suppose data processing system **100** is divided into three logical partitions, P1, P2, and P3. Each of I/O adapters **120-121**, **128-129**, **136**, and **148-149**, each of processors **101-104**, and each of local memories [160-164] 160-163 is assigned to one of the three partitions. For example, processor **101**, memory **160**, and I/O adapters **120, 128, and 129** may be assigned to logical partition P1; processors **102-103**, memory **161**, and I/O adapters **121** and **136** may be assigned to partition P2; and processor **104**, memories **162-163**, and I/O adapters **148-149** may be assigned to logical partition P3.

Amended paragraph commencing on page 8, line 13:

Each operating system executing within data processing system **100** is assigned to a different logical partition. Thus, each operating system executing within data processing system **100** may access only those I/O units that are within its logical partition. Thus, for example, one instance of the Advanced Interactive Executive (AIX) operating system may be executing within partition P1, a second instance (image) of the AIX operating system may be executing within partition P2, and a Windows 2000 operating system may be operating within logical partition [P1] P3. Windows 2000 is a product and trademark of Microsoft Corporation of Redmond, Washington.

Amended paragraph commencing on page 8, line 26:

Peripheral component interconnect (PCI) Host bridge **114** connected to I/O bus **112** provides an interface to PCI local bus **115**. A number of Input/Output adapters **120-121** may be connected to PCI bus **115** by a PCI bus **118** and **119** and EADS (PCI-PCI bridge) **116**. Typical PCI bus implementations will support between four and eight I/O

adapters (i.e. expansion slots for add-in connectors). Each I/O [Adapter] adapter **120-121** provides an interface between data processing system **100** and input/output devices such as, for example, other network computers, which are clients to data processing system **100.**

Amended paragraph commencing on page 9, line 6:

An additional PCI host bridge **122** [provide] provides an interface for an additional PCI bus **123**. PCI bus **123** is connected to a plurality of PCI I/O adapters **128-129** by a PCI bus **126-127** and EADS **124**. Thus, additional I/O devices, such as, for example, modems or network adapters may be supported through each of PCI I/O adapters **128-129**. In this manner, data processing system **100** allows connections to multiple network computers.

Amended paragraph commencing on page 9, line 20:

A PCI host bridge **130** provides an interface for a PCI bus **131** to connect to I/O bus **112**. PCI bus **131** connects PCI host bridge **130** to the service processor mailbox interface and ISA bus access pass-through logic **194** and EADS **132**, which is coupled to PCI I/O adapter **136** through PCI bus **133**. The ISA bus access pass-through logic **194** forwards PCI accesses destined to the PCI/ISA bridge **193**. The NV-RAM storage **192** is connected to the ISA bus **196**. The Service processor **135** is coupled to the service processor mailbox interface **194** through its local PCI bus **195**. Service processor **135** is also connected to processors **101-104** via a plurality of JTAG/I^2C buses **134**. JTAG/I^2C buses **134** are a combination of JTAG/scan busses (see IEEE 1149.1) and Phillips I^2C busses. However, alternatively, JTAG/I^2C buses **134** may be replaced by only Phillips I^2C busses or only JTAG/scan busses. All SP-ATTN signals of the host processors **101, 102, 103,** and **104** are connected together to an interrupt input signal of the service processor. The service processor **135** has its own local memory **191**, and has access to the hardware op-panel **190**.

Amended paragraph commencing on page 11, line 30:

With reference now to **Figure 2**, a block diagram of an exemplary logically partitioned platform is depicted in which the present invention may be implemented. The hardware in logically partitioned platform **200** may be implemented as, for example, server **100** in **Figure 1**. Logically partitioned platform **200** includes partitioned hardware **230**, Open Firmware (OF) **210** including Kernal **212**, and operating systems **202-208**. Operating systems **202-208** may be multiple copies of a single operating system or multiple heterogeneous operating systems simultaneously run on platform **200**.

Amended paragraph commencing on page 12, line 10:

Partitioned hardware **230** includes a plurality of processors **232-238**, a plurality of system memory units **240-246**, a plurality of input/output (I/O) adapters **248-262**, and a storage unit **270**. Each of the processors [**242-248**] **232-238**, memory units **240-246**, NV-RAM storage **298**, and I/O adapters **248-262** may be assigned to one of the multiple partitions within logically partitioned platform **200**, each of which corresponds to one of operating systems **202-208**.

Amended Abstract of the Disclosure commencing on page 25, line 8:

A [method,] system[, and apparatus] for managing input/output drawers within a data processing system [is provided]. [In one embodiment, a service processor assigns a] A unique [location] identifier is assigned to each of a plurality of [input/output] drawers[. Each of these unique location identifiers is stored in memory. The unique location identifier] , and is used by the operating system to identify the [input/ouput] drawers in the system regardless of how these [input/output] drawers are interconnected [by cables]. [In this embodiment, the system firmware assigns another] Another unique PCI-bridge identifier is assigned to each of a plurality of PCI Host bridges (PHBs) from all [input/output] drawers[. The unique PCI-bridge identifier] , and is used by the operating system to perform input/output processes to [input/output] devices associated with the

plurality of [PCI Host bridges from all input/output drawers] PHBs such that the [operating systems] ODM object for each of the [PCI Host bridges from an I/O drawer] PHBs remains the same regardless of how the [I/O] drawer is interconnected in the system. When a new [input/output] drawer is added to the [data processing] system, [the service processor assigns] a new unique [location] identifier is assigned to the new [input/output] drawer ensuring that the unique [location] identifiers previously assigned to the other [I/O] drawers are not used to identify the new [I/O] drawer.

Amended Claims:

1. (Amended) A method of managing input/output drawers within a data processing system, the method comprising:

assigning a unique [location] identifier to each of a plurality of input/output drawers; and

storing the unique [location] identifier in memory;

wherein the unique [location] identifier is used by [the] an operating system to identify the plurality of input/output drawers regardless of how the input/output drawers are interconnected by cables, such that addresses used when accessing devices contained within said plurality of input/output drawers do not change when reconfiguring at least one of the input/output drawers within the data processing system.

2. (Amended) The method as recited in claim 1, further comprising:

responsive to a determination that a new input/output drawer has been added to the data processing system, assigning a new unique [location] identifier to the new input/output drawer, wherein the new unique [location] identifier is different from any of the unique [location] identifiers previously assigned, such that each of the plurality of input/output drawers maintains the same unique [location] identifier.

4. (Amended) The method as recited in claim 2, wherein the unique [location] identifier and the new unique [location] identifier are stored in a device tree.

5. (Amended) The method as recited in claim 2, wherein the unique [location] identifier comprise device nodes and location codes.

8. (Amended) A computer program product in a computer readable media for use in a data processing system for managing input/output drawers within the data processing system, the computer program product comprising:

first instructions for assigning a unique [location] identifier to each of a plurality of input/output drawers; and

second instructions for storing the unique [location] identifier in memory;

wherein the unique [location] identifier is used by [the] an operating system to identify the plurality of input/output drawers regardless of how the input/output drawers are interconnected by cables, such that addresses used when accessing devices contained within said plurality of input/output drawers do not change when reconfiguring at least one of the input/output drawers within the data processing system.

9. (Amended) The computer program product as recited in claim 8, further comprising:

third instructions, responsive to a determination that a new input/output drawer has been added to the data processing system, for assigning a new unique [location] identifier to the new input/output drawer, wherein the new unique [location] identifier is different from any of the unique [location] identifiers previously assigned, such that each of the plurality of input/output drawers maintains the same unique [location] identifier.

10. (Amended) The computer program product as recited in claim 8, wherein said first and second instructions [comprising the computer program product] are executed in a service processor.

11. (Amended) The computer program product as recited in claim 9, wherein the unique [location] identifier and the new unique [location] identifier are stored in a device tree.

12. (Amended) The computer program product as recited in claim 9, wherein the unique [location] identifier comprise device nodes and location codes.

15. (Amended) A system for managing input/output drawers within a data processing system, the system comprising:

first means for assigning a unique [location] identifier to each of a plurality of input/output drawers; and

second means for storing the unique [location] identifier in memory;

wherein the unique [location] identifier is used by [the] an operating system to identify the plurality of input/output drawers regardless of how the input/output drawers are interconnected by cables, such that addresses used when accessing devices contained within said plurality of input/output drawers do not change when reconfiguring at least one of the input/output drawers within the data processing system.

16. (Amended) The system as recited in claim 15, further comprising:

third means, responsive to a determination that a new input/output drawer has been added to the data processing system, for assigning a new unique [location] identifier to the new input/output drawer, wherein the new unique [location] identifier is different from any of the unique [location] identifiers previously assigned, such that each of the plurality of input/output drawers maintains the same unique [location] identifier.

17. (Amended) The system as recited in claim 15, wherein said first and second means [comprising the system] are executed in a service processor.

18. (Amended) The system as recited in claim 16, wherein the unique [location] identifier and the new unique [location] identifier are stored in a device tree.

19. (Amended) The system as recited in claim 16, wherein the unique [location] identifier comprise device nodes and location codes.